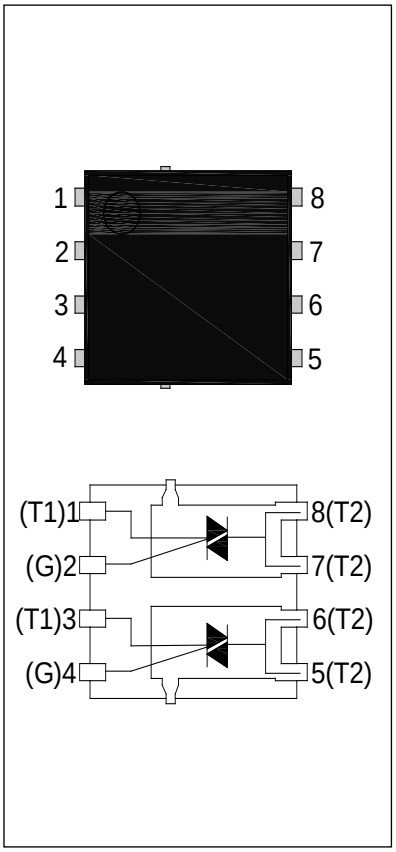
JST04G-800SWD 4A TRIAC

Rev.A.1.0

DESCRIPTION:

The JST04G-800SWD contains two independent triacs. It is suitable for general purpose AC switching. It can be used as an ON/OFF function in applications such as heating regulation, induction motor starting circuits, for phase control operation in light dimmers, motor speed controllers, Mahjong machines, fans. JST04G-800SWD snubberless triac is especially recommended for use on inductive loads. It can be driven directly through the MCU I/O port. Package DFN5*6-8L is RoHS compliant.



MAIN FEATURES

Symbol	Value	Unit
$I_{T(RMS)}$	4	A
V_{DRM} /V_{RRM}	800	V
$I_{GT\ I\ /\ II/III}$	10/10/10	mA

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Storage junction temperature range	T_{stg}	-40-150	℃
Operating junction temperature range	T_j	-40-125	℃
Repetitive peak off-state voltage (T_j=25℃)	V_{DRM}	800	V
Repetitive peak reverse voltage (T_j=25℃)	V_{RRM}	800	V
RMS on-state current (T_C≤45℃)	$I_{T(RMS)}$	4	A
Non repetitive surge peak on-state current (full cycle , t_p=20ms , T_j=25℃)	I_{TSM}	40	A
Non repetitive surge peak on-state current (full cycle , t_p=16.6ms , T_j=25℃)		44	
I^2t value for fusing (t_p=10ms , T_j=25℃)	I^2t	8	A^2s
Critical rate of rise of on-state current (I_G=2×I_{GT} , f=100Hz , T_j=125℃)	dI/dt	50	A/μs
Peak gate current (t_p=20μs , T_j=125℃)	I_{GM}	4	A

Average gate power dissipation (T_j=125℃)	$P_{G(AV)}$	0.5	W
Peak gate power	P_{GM}	10	W
Peak pulse voltage (T_j=25℃; non-repetitive,off-state;FIG.8)	V_{pp}	3.5	kV

ELECTRICAL CHARACTERISTICS (T_j=25℃ unless otherwise specified)

Symbol	Test Condition	Quadrant	Value		Unit
I_{GT}	V_D =12V R_L =33Ω	Ⅰ-Ⅱ-Ⅲ	MAX.	10	mA
V_{GT}		Ⅰ-Ⅱ-Ⅲ	MAX.	1	V
V_{GD}	V_D =V_{DRM} T_j =125℃ R_L =3.3KΩ	Ⅰ-Ⅱ-Ⅲ	MIN.	0.2	V
I_L	I_G =1.2I_{GT}	Ⅰ-Ⅲ	MAX.	20	mA
		Ⅱ		35	
I_H	I_T =100mA		MAX.	15	mA
dV/dt	V_D=540V Gate Open T_j =125℃		MIN.	1000	V/μs
(dI/dt)c	(dV/dt)c=10V/μs, Tj=125℃		MIN.	2.5	A/ms
t_{on}	I_G=20mA I_A=200mA I_R=20mA T_j=25℃		TYP.	2.5	μs
t_{off}				25	

STATIC CHARACTERISTICS

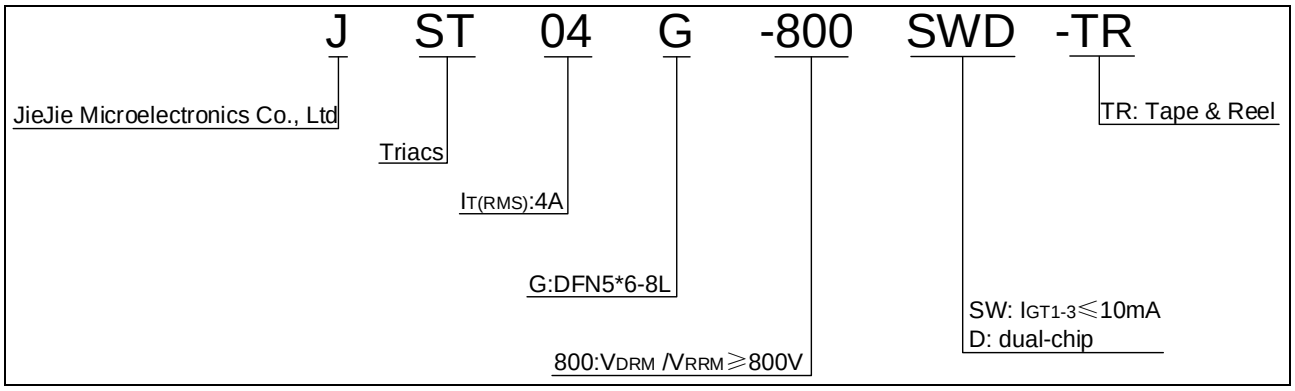
Symbol	Parameter		Value(MAX.)	Unit
V_{TM}	I_{TM} =5A t_p=380μs	T_j=25℃	1.4	V
V_{TO}	Threshold voltage	T_j=125℃	0.8	V
R_D	Dynamic resistance	T_j=125℃	66	mΩ
I_{DRM}	V_D =V_{DRM} V_R =V_{RRM}	T_j=25℃	5	μA
I_{RRM}		T_j=125℃	0.25	mA

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	junction to case (AC)	15	℃/W
$R_{th(j-a)}$	junction to ambient (AC)	65	℃/W

*Note： Testing one of the chips to obtain the value of $R_{th(j-c)}$ and $R_{th(j-a)}$.

ORDERING INFORMATION



MARKING

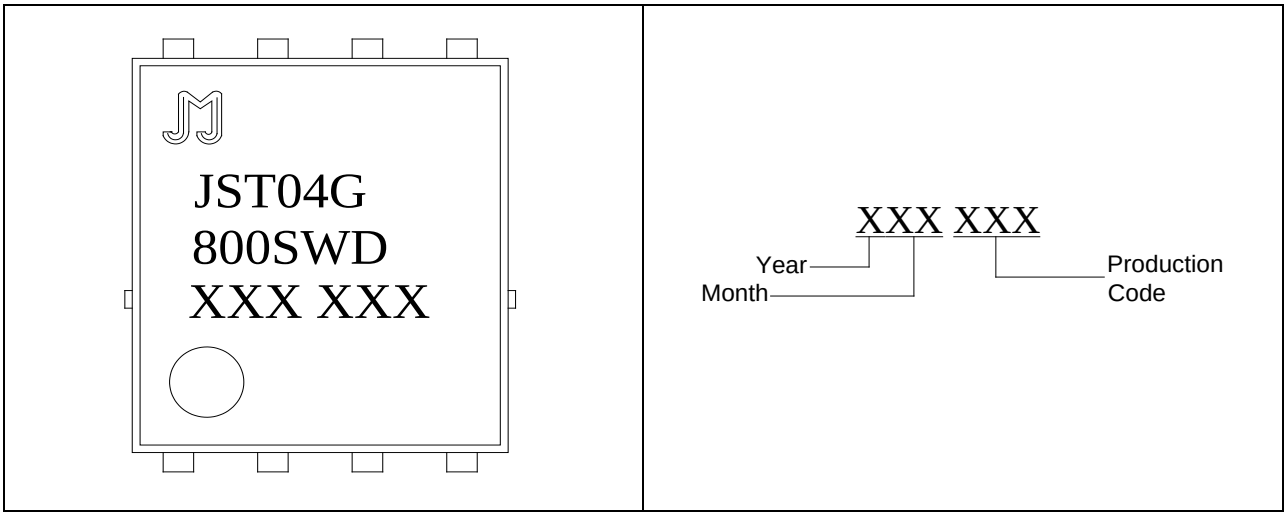


FIG.1 Maximum power dissipation versus RMS on-state current

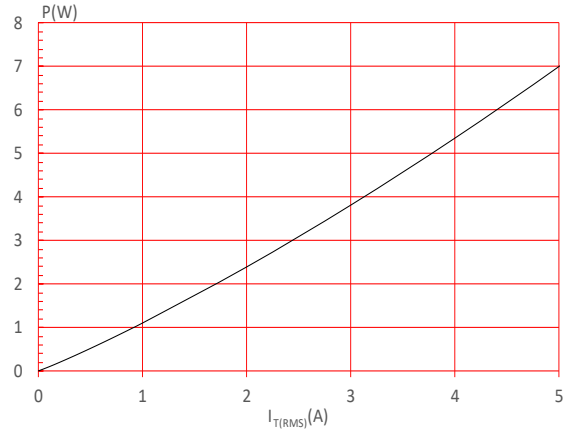


FIG.2: RMS on-state current versus case temperature

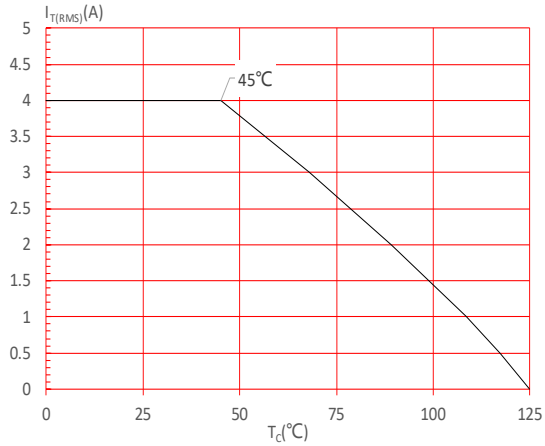


FIG.3: RMS on-state current versus ambient temperature (printed circuit board FR4,copper thickness:35μm)(full cycle)

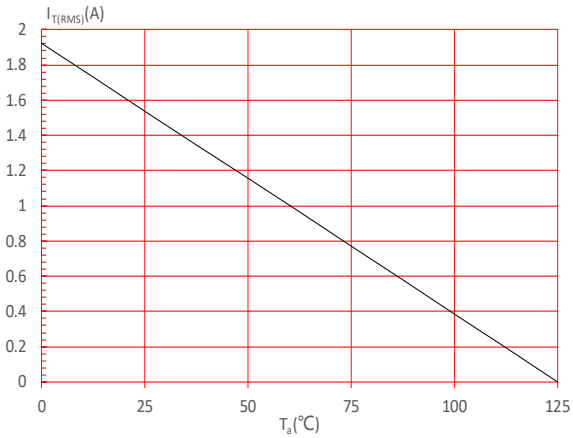


FIG.4: Surge peak on-state current versus number of cycles

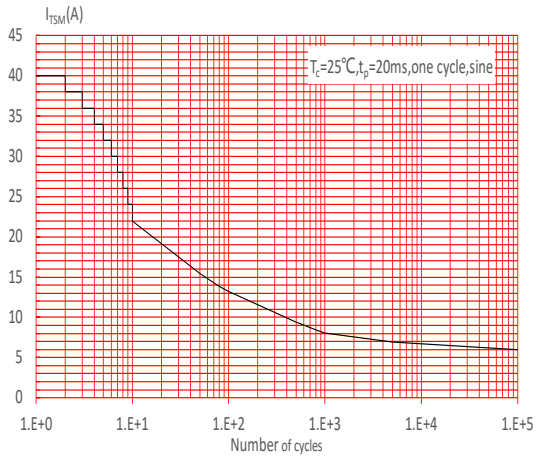


FIG.5: On-state characteristics

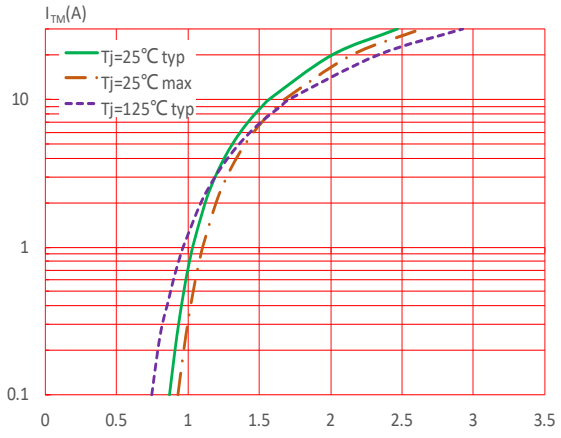


FIG.6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width t_p<20ms, and corresponding value of I^2t (dI/dt<50A/μs)

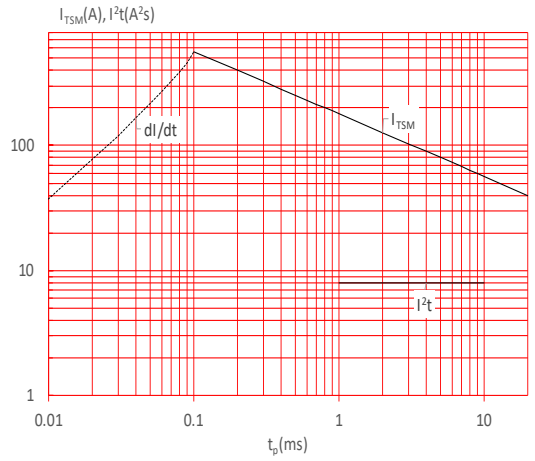


FIG.7: Relative variations of gate trigger current, holding current and latching current versus junction temperature

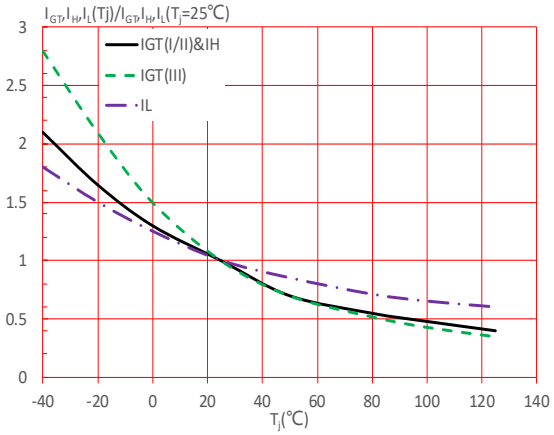
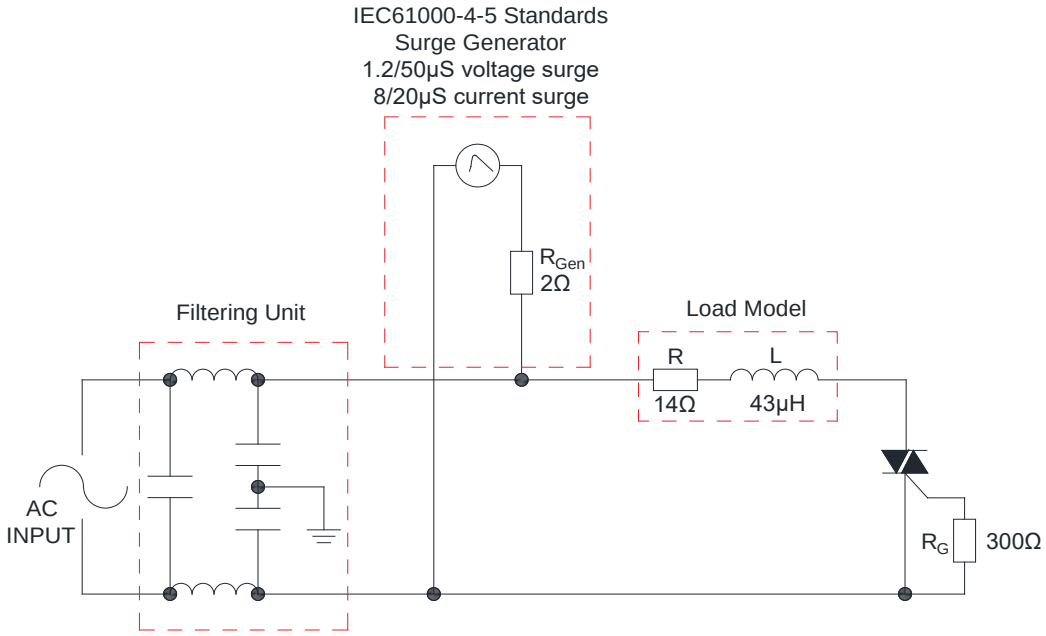
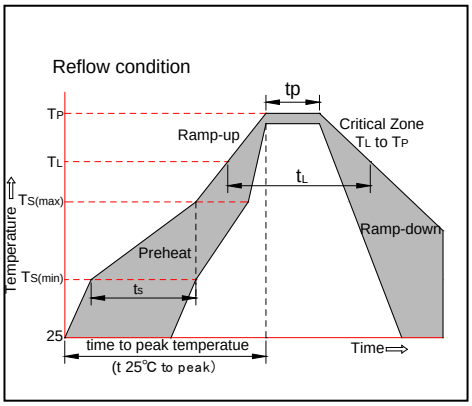


FIG.8：Test circuit for inductive and resistive loads to IEC-61000-4-5 standards



SOLDERING PARAMETERS

Reflow Condition		Pb-Free assembly (see figure at right)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150℃
	-Temperature Max($T_{s(max)}$)	+200℃
	-Time (Min to Max) (ts)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L)to peak)		3℃/sec. Max
$T_{s(max)}$ to T_L - Ramp-up Rate		3℃/sec. Max
Reflow	-Temperature(T_L) (Liquidus)	+217℃
	-Temperature(t_L)	60-150 secs.
Peak Temp (T_p)		+260(+0/-5)℃
Time within 5℃of actual Peak Temp (t_p)		20-40secs.
Ramp-down Rate		6℃/sec. Max
Time 25℃ to Peak Temp (T_P)		8 min. Max
Do not exceed		+260℃



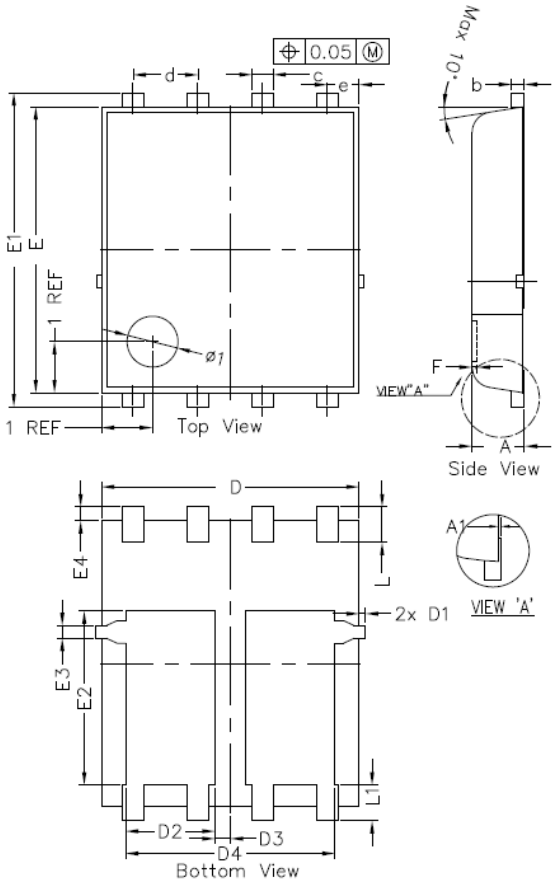
ORDERING INFORMATION

Order code	Voltage V_{DRM}/V_{RRM} (V)	IGT(mA)	Package	Base qty. (pcs)	Delivery mode
		Ⅰ-Ⅱ-Ⅲ			
JST04G-800SWD-TR	800	10	DFN5*6-8L	5000	Tape & Reel

Document Revision History

Date	Revision	Changes
Aug.01, 2023	A.1.0	Last updated

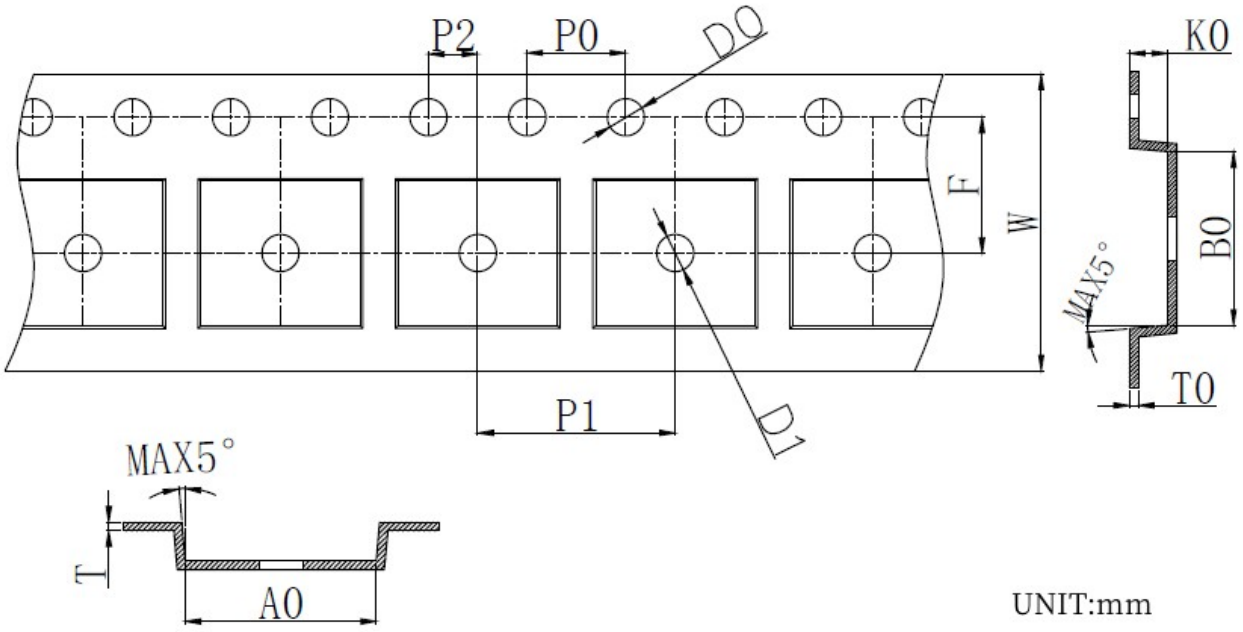
PACKAGE MECHANICAL DATA



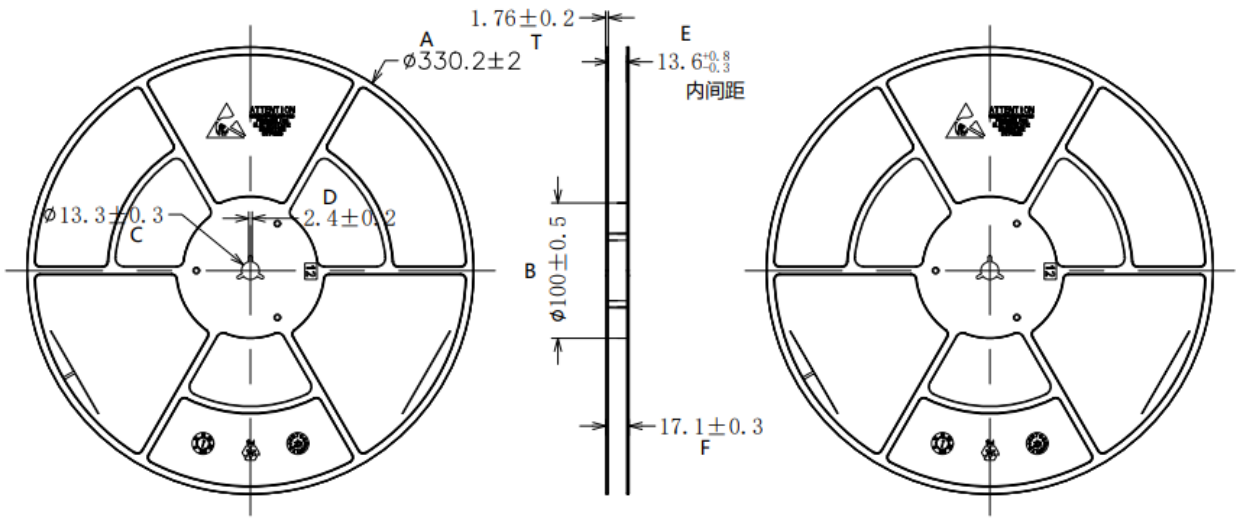
SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
* A	0.900	1.000	1.100	0.035	0.039	0.043
A1	0.000	---	0.050	0.000	----	0.002
b	0.246	0.254	0.312	0.010	0.010	0.012
* c	0.310	0.410	0.510	0.012	0.016	0.020
d		1.27 BSC			0.050 BSC	
* D	4.950	5.050	5.150	0.195	0.199	0.203
⚠ *D1	---	---	0.125	---	---	0.005
*D2	1.650	1.750	1.850	0.065	0.069	0.073
D3	0.200	0.300	0.400	0.008	0.012	0.016
D4	4.000	4.100	4.200	0.157	0.161	0.165
e		0.62 BSC			0.024 BSC	
* E	5.500	5.600	5.700	0.217	0.220	0.224
* E1	6.050	6.150	6.250	0.238	0.242	0.246
E2	3.310	3.410	3.510	0.130	0.134	0.138
E3	0.150	0.250	0.350	0.006	0.010	0.014
* E4	0.175	0.275	0.375	0.007	0.011	0.015
F	-	-	0.100	-	-	0.004
⚠ * L	0.500	0.600	0.700	0.02	0.02	0.03
L1	0.600	0.700	0.800	0.02	0.03	0.03

NOTE:
1. PACKAGE BODY SIZE EXCLUDE MOLD FLASH AND GATE BURR.
   MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 5 MIL EACH SIDE.
2. CONTROLLING DIMENSION IS MILLIMETER, INCH FOR REFERENCE ONLY.

DELIVERY MODE



SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	6.60±0.10	5.50±0.10	1.30±0.10	4.00±0.10	8.00±0.10	2.00±0.05
SYMBOL	T	E	F	D0	D1	W
SPEC	0.25±0.03	1.75±0.10	5.50±0.10	1.55±0.05	1.55±0.10	12.00 $^{+0.3}_{-0.1}$



A±2	B±0.5	C±0.3	D±0.2	E +0.8 -0.3	F±0.3	T±0.2
330.2	ø100	ø13.3	2.4	13.6	17.1	1.76

PACKAGE	OUTLINE	REEL (PCS)	PER CARTON (PCS)	TAPE & REEL
DFN5*6-8L	TAPING	5,000	50,000	13 inch

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