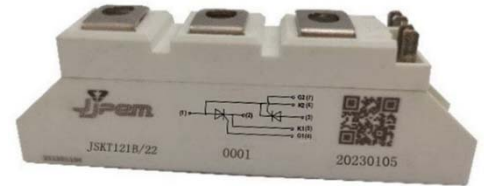


JSKT121B/22

Description

- 1) A package of series of two chips.
- 2) With high thermal conductivity DBC as the insulation.
- 3) Welding by vacuum welding technology, which provide high reliability.



Typical Application

DC motor control, temperature control and light control system.

Absolute Maximum Ratings (Packaged into modules, unless otherwise specified, $T_{CASE}=25^{\circ}C$)

Parameter	Test Conditions	Symbol	Values	Unit
Operating junction temperature range		T_j	-40-125	$^{\circ}C$
Storage temperature range		T_{stg}	-40-125	$^{\circ}C$
Repetitive peak off-state voltage	$T_j=25^{\circ}C$	V_{DRM}	2200	V
Repetitive peak reverse voltage	$T_j=25^{\circ}C$	V_{RRM}	2200	V
Non-repetitive peak off-state voltage	$T_j=25^{\circ}C$	V_{DSM}	2300	V
Non-repetitive peak reverse voltage	$T_j=25^{\circ}C$	V_{RSM}	2300	V
Average on-state current	$T_C=85^{\circ}C$	$I_{T(AV)}$	120	A
Peak on-state surge current	$t_P=10ms$ $V_R=0.6V_{RRM}$	I_{TSM}	2700	A
I^2t value for fusing	$t_P=10ms$ $V_R=0.6V_{RRM}$	I^2t	36500	A^2s
Critical rate of rise of on-state current	$I_G=2 \times I_{GT}$	di/dt	150	$A/\mu s$
Isolation voltage	A.C 50Hz(1s/1min)	V_{ISO}	3600/3000	V

Electrical Characteristics (Packaged into modules, unless otherwise specified, $T_{CASE}=25^{\circ}C$)

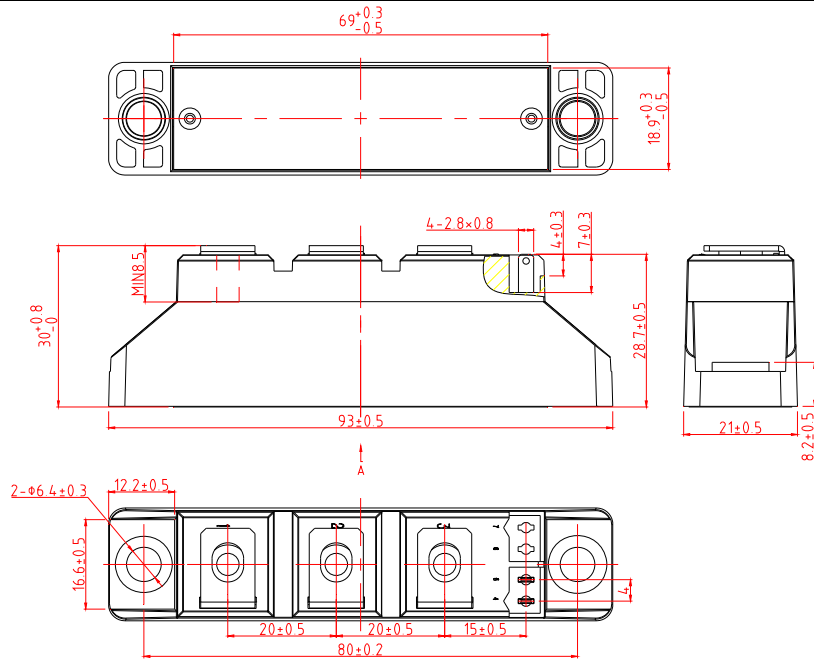
Parameter	Test Conditions	Symbol	Values	Unit
Peak on-state voltage	$I_T=360A$ $t_P=380\mu s$	V_{TM}	≤ 1.8	V
Threshold voltage	$T_j=125^{\circ}C$	V_{TO}	≤ 0.95	V
Dynamic resistance	$T_j=125^{\circ}C$	R_d	≤ 2.1	$m\Omega$
Repetitive peak off-state current	$V_D=V_{DRM}$ $T_C=25^{\circ}C$	I_{DRM1}	≤ 100	μA
	$T_C=125^{\circ}C$	I_{DRM2}	≤ 40	mA



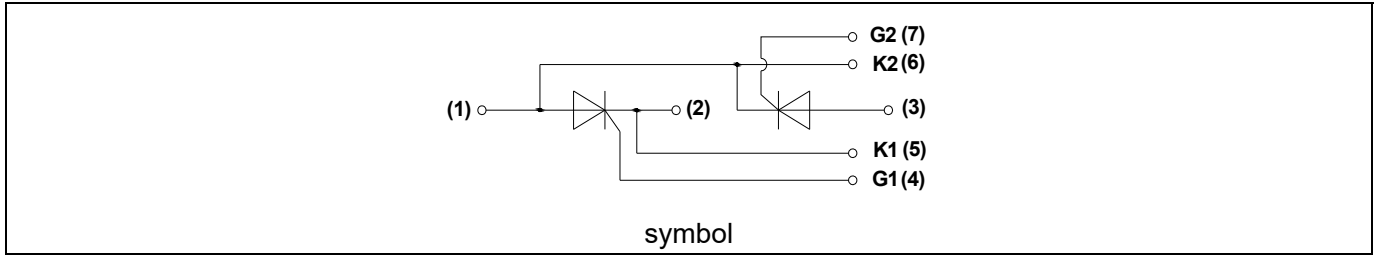
Repetitive peak reverse current	$V_R=V_{RRM}$ $T_C=25^\circ\text{C}$ $T_C=125^\circ\text{C}$	I_{RRM1} I_{RRM2}	≤ 100 ≤ 40	μA mA
Triggering gate current	$V_D=12\text{V}$ $R_L=30\Omega$	I_{GT}	20-120	mA
Holding current	$I_T=1\text{A}$	I_H	≤ 250	mA
Latching current	$I_G=1.2I_{GT}$	I_L	≤ 300	mA
Triggering gate voltage	$V_D=12\text{V}$ $R_L=30\Omega$	V_{GT}	≤ 1.8	V
Non triggering gate voltage	$V_D=V_{DRM}$ $T_j=125^\circ\text{C}$	V_{GD}	≥ 0.25	V
Critical rate of rise of voltage	$V_D=2/3V_{DRM}$ $T_j=125^\circ\text{C}$ Gate Open	dv/dt	≥ 1000	V/ μs
Thermal resistance	Junction to case Case to heatsink	$R_{th(j-c)}$ $R_{th(c-s)}$	0.29 0.21	$^\circ\text{C/W}$

Mechanical Characteristics

Module size	93mm×21mm
Module height	30mm
Terminal distance of (1) /(2) /(3)	20mm
Mounting torque(M5)	$5\pm 15\%\text{Nm}$
Terminal torque(M5)	$3\pm 15\%\text{Nm}$



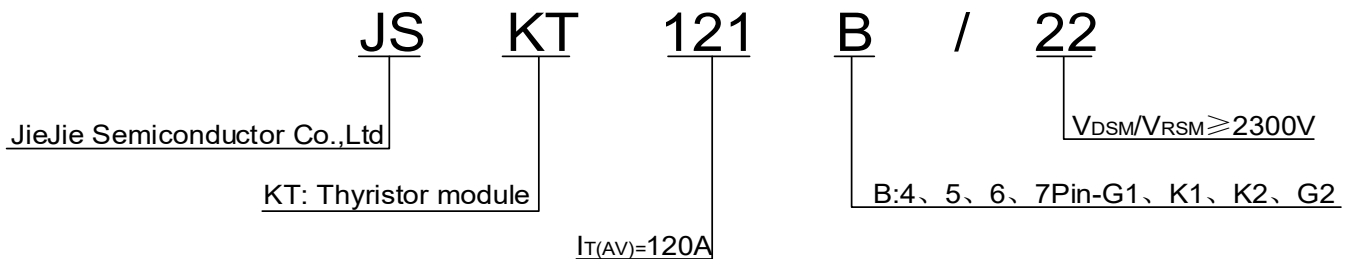
T1



Instructions and Precautions

- 1) There is no severe vibration and shock in operating environment, and there should be no impurity and atmosphere which may corrode metal and damage the insulation in the air-dielectric.
- 2) The operating condition of the product can't out of range of the above parameters.
- 3) When the product is installed on the radiator, the radiator's surface should be confirmed flat, smooth, wipe clean with alcohol, and coated evenly with a layer of thermal grease which thickness is moderate on the contact surface between product and radiator. When the module is fastened on the surface of the radiator, the M5 or M6 screws and spring washers are used and fastened with 5NM torque. After the module is operated 1 hour, all screws must be refastened.
- 4) The connection with the main electrode of module can use copper, welding, socket and so on. The contact surface should be smooth and flat, which make good contact. While the connection with the control electrode of module is installed, attention should be paid to the corresponding connection of each pin. After the completion of the connection, do not plug and pull out the lead of the control electrode freely.

Ordering Information



Performance Curves

FIG.1: Power dissipation vs. on-state current (per thyristor)

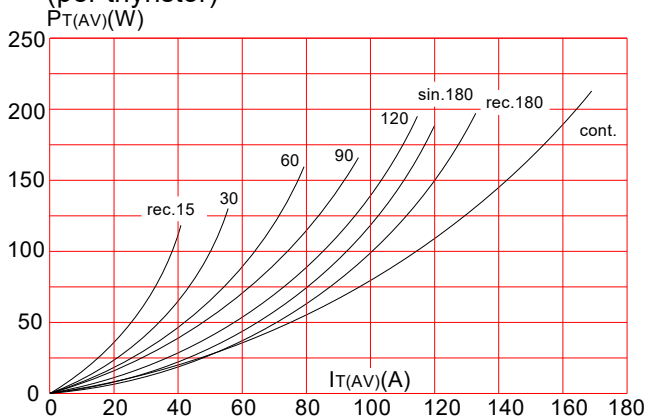


FIG.2: Maximum transient thermal impedance junction to case(per thyristor)

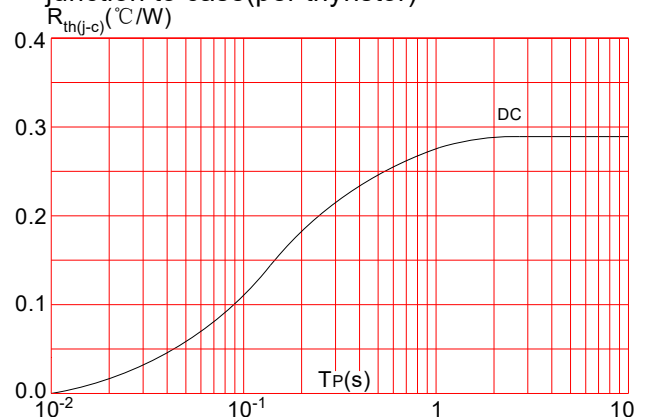




FIG.3:Forward characteristics
(per thyristor)

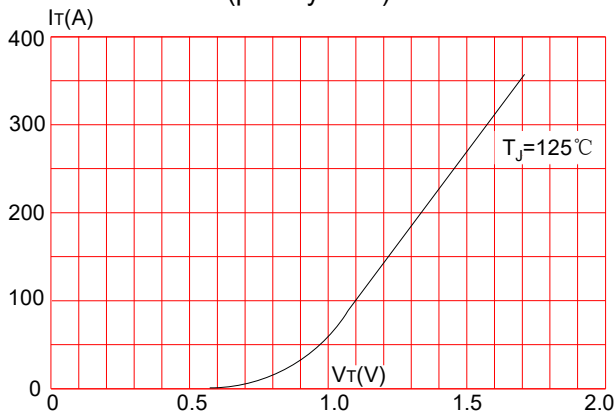
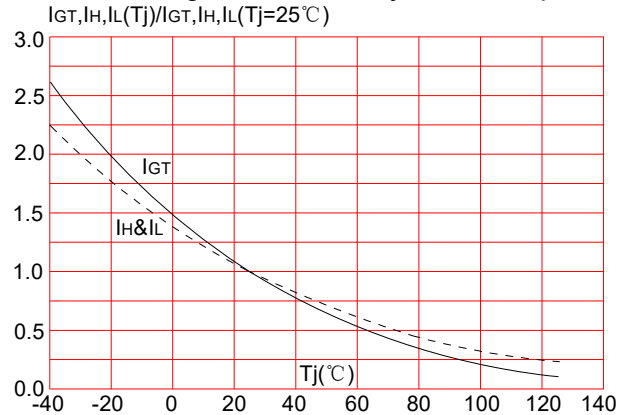


FIG.4: Relative variations of gate trigger current, holding current and latching current versus junction temperature




Information furnished in this document is believed to be accurate and reliable. However, JieJie Semiconductor Co., Ltd. assumes no responsibility for the consequences of use without consideration for such information nor use beyond it.

Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, JieJie complies with the agreement.

Products and information provided in this document have no infringement of patents. JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.

This document is the third version which is made in 28-Aug.-2024. This document supersedes and replaces all information previously supplied.

 is registered trademarks of JieJie Semiconductor Co., Ltd. Copyright©2024 Semiconductor Co., Ltd. Printed All rights reserved.